Applications of Commercial Semiconductor Technologies in Space Systems

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Abstract -Key issues are discussed that must be overcome in order to apply commercial semiconductor technologies in space, emphasizing ways to test and qualify devices so they meet radiation hardness requirements. Three examples are shown, including a microprocessor, advanced memory technologies, and a high-precision analog-to-digital converter. The effects of advanced processing and scaling on radiation hardness are also discussed.

Introduction

There is increasing interest in the use of unhardened commercial electronics technologies in space systems because of the higher performance, lower direct semiconductor cost, and advanced levels of integration that commercial technologies provide. These advantages are partially offset by increased radiation testing and hardness assurance costs, compared to hardened technologies, along with the risk that process changes in commercial technologies may inadvertently compromise the radiation hardness. This paper discusses three examples of commercial technology insertion in space, including advanced memory technologies, a microprocessor, and high-precision analog-to-digital converters. Data will be presented showing how total dose and single-particle effects affect these devices, and how part selection, hardness assurance, and system design techniques were used to allow them to be applied in space.

Radiation Environment

There are three primary components of the natural space environment. First, high-energy protons and electrons are trapped by planetary magnetic fields to form belts, such as the Earth's Van Allen belts. Satellites are subjected to large fluxes of these particles when they pass through the radiation belts. Second, galactic cosmic rays occur everywhere in space. These are highly energetic particles with a wide range of atomic numbers. The flux rate is very low compared to the number of particles in the radiation belts. However, a single galactic cosmic ray can deposit sufficient charge in a modern integrated circuit transistor (o change the state of internal storage elements, and may also cause more complex behavior, such as latchup. Third, solar flares produce varying quantities of electrons, protons, and lower energy charged particles. Solar flare activity varies widely at different times, and very high fluxes of particles may occur over time periods of hours or days during periods of high solar activity. Table 1 summarizes the three components of the natural space environment, along with their primary effects on CMOS devices.

Effects of Radiation on MOS Devices

Although bipolar devices are used in some key integrated circuit technologies, MOS is the dominant technology for modern integrated circuits, and therefore will be the main focus of this paper. Two basic effects occur when MOS devices are exposed to space radiation: *ionization damage*, which is a semi-permanent effect that occurs when charge produced within oxides builds up at semiconductor/oxide interfaces; and *single-particle effects*, which are circuit-related effects caused by the short-duration charge transients that are produced withi n the semiconductor region by interaction of heavy particles.

Table 1. Summary of Space Radiation Environments and "I'heir Effects on CMOS Devices

Radiation Source	Particle Types	Primary Effects in Devices
Trapped Radiation Belts	Electrons	Ionization damage
	Protons	Ionization damage; single-event effects (SEE) in sensitive devices
Galactic Cosmic Rays	High-energy charged particles	SEE
Solar Flares	Electrons	Ionization damage
	Protons	Ionization damage; SEE in sensitive devices
	Lower energy heavy charged particles	SEE

Ionization Damage

Total dose refers to the amount of energy deposited in a material (such as a semiconductor or insulator) through ionization processes when energetic particles pass through the material. The unit used to specify deposited energy is the rad, which is defined as 100 ergs/g of material. Total dose levels encountered by satellites and space probes are typically between 10 and. 100 krad(Si), although systems exist with requirements above and below this range. Trapped electrons and protons in the Earth's radiation belts and solar flare particles are the main cause of ionization damage. Relatively small amounts of shielding can be used to reduce total dose levels inside satellites.

Ionization produces electron-hole pairs within insulators and semiconductors. Ionization damage in MOS devices depends on the way that electrons and holes are transported and trapped at the silicon-silicon dioxide interface. The net effect of ionizing radiation on MOS device oxides depends upon the oxide thickness, the field applied to the oxide during and after exposure, and trapping and recombination within the oxide. The latter factor is strongly affected by processing techniques during manufacture.

Bias conditions strongly influence total dose degradation.[1] A positive gate-to-silicon oxide field will cause holes to be transported to the silicon-silicon dioxide interface, where some fraction of them will be trapped, whereas a negative field will cause the holes to be transported to the gate, where they recombine with electrons and do not create trapped holes. For n-channel devices, this worst-case condition for hole transport and trapping requires positive voltage at the gate relative to the source (device biased on), For p-channel devices the worst-case condition is negative gate -to-source voltage, with the device biased off.

Holes trapped at the silicon-silicon dioxide interface change the threshold voltage. For n-channel devices, trapped holes decrease the threshold voltage, and cause a transistor to gradually shift towards depletion mode as the total dose increases, as shown in Figure 1. For p-channel devices, hole traps cause the devices to shift further in the enhancement (off) direction, as shown in the lower curves of Figure 1, Present commercial CMOS technologies usually fail at levels between 10 and 50 krad(Si).

In practice, total dose effects in MOS devices are much more complicated than the elementary description of hole trapping described above. Three additional factors have to be taken into account :

Annealing. The trapped holes are not stable, but gradually anneal with time. The rate of annealing depends on the oxide properties, and are related to the specific manufacturing process. Substantial recovery may occur over time periods of days to months. This

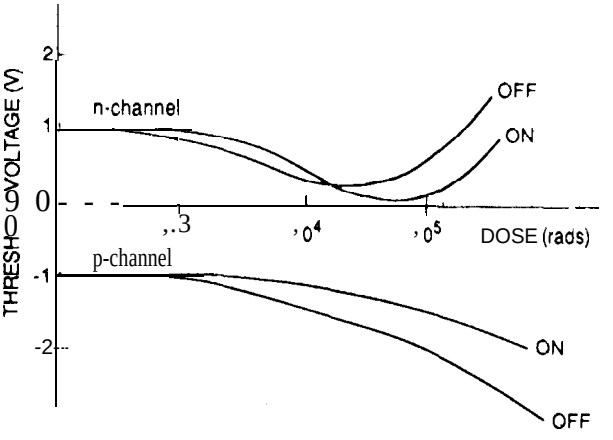

Figure 1. Threshold voltage shift for n- and p-channel transistors in a typical commercial process

has a major effect on the interpretation of laboratory test results for space environments, which are usually concerned with very low dose rates. In some cases, annealing allows devices to be used at much higher radiation levels in space because much of the damage anneals during the life of the satellite. However, as discussed below, interface traps must also be accounted for when using this approach.

Interface Traps. A second charge component, interface traps, also occurs when MOS devices are exposed to ionizing radiation. Interface traps behave differently in n- and p-channel devices, For n-channel devices, the interface traps shift the threshold voltage in the opposite direction from trapped holes, whereas the threshold shift from interface traps is in the same direction as that of trapped holes for p-channel devices. Interface traps also degrade mobility, which affects switching time.

In n-channel devices, interface traps can partially compensate the threshold shift from trapped holes because the two charge components have opposite signs. If the number of interface traps is a significant fraction of the hole traps, the net effect at long times is a *positive* shift in threshold voltage due to the fact that most of the holes anneal (interface traps do not anneal at normal temperatures). This effect, called *rebound* in the literature, severely complicates total dose testing because the interface traps may compensate the negative threshold shift of the trapped holes, making devices appear much harder to radiation under certain combinations of dose and time.[2,3]

Field Oxides. Finally, all MOS devices have a thick field oxide. The parasitic field oxide transistor must remain turned off in order for MOS devices to function properly. If ionizing radiation causes this transistor to invert, large increases in leakage current will occur, and the circuit will fail. [4] *This is a very important failure mode for commercial CMOS devices, and usually*

dominates devices with feature sizes below 2 μm. Figure 2 shows the effect of field oxide inversion on the 1-V characteristics of a 1.2 μm commercial CMOS process. Hardened processes use special processing techniques to reduce field oxide effects.

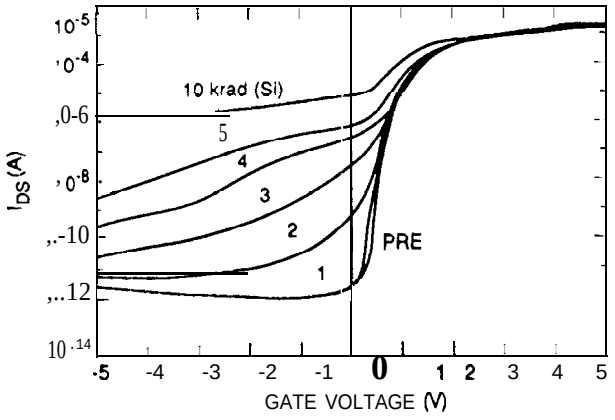

Figure 2. Effect of field-oxide inversion on I-V characteristics of an n-channel MOS transistor.

SEU Charge Collection and Error Rates

Charge Generation and Collection. High-energy protons or heavy ions deposit a dense track of electron-hole pairs through ionization loss when they pass through p-n junctions. The net effect is a very short duration pulse of current that induces transient charges at internal circuit nodes, The magnitude of the charge depends on the energy and ion type, as well as the path length over which the charge is collected, and is generally much larger for ions with high atomic number. [s,6] The prompt charge is collected in less than 1 ns, which is shorter than the response time of most MOS transistors.

The effect of these random charges on the circuit depends on a number of factors, including the minimum charge required to switch a digital circuit. If the energy deposited by the ion exceeds the minimum charge (critical charge), then the circuit will be upset or otherwise affected by the passage of the ion.

A number of effects can be induced by high-energy particles. [7] Not all of these effects are possible in all devices, either because the critical charge for the effect is too high, or because the specific design (or processing) of the circuit precludes the occurrence (e.g., latchup cannot occur in silicon-on-insulator technology). These effects can be subdivided into two basic categories:

(1) Transient effects, such as single-event upset (SEU) and multiple-bit upset that change the state of internal storage elements, but can be reset to normal operation by a series of electrical operations or reinitialization; and

(2) Potentially catastrophic events, such as single-event latchup (SF.].) that may cause destruction unless they are detected and corrected for within a short time after they occur.

Units and Environmental Specification. The charge produced by a heavy particle within a semiconductor is called linear energy transfer (LET). LET is the energy transferred per unit length , normalized to the material density. It is expressed in MeV-cm^2/mg. For silicon, it is approximately 100 times greater than the charge deposition density in pC/μm. The charge collected at internal circuit nodes is directly proportional to LET. The galactic cosmic ray environment consists of a distribution of different particle types with different ion species and energies. The number of particles falls off rapidly with increasing LET. There are very few particles with LET > 26 MeV-cm^2/mg, the so-called iron threshold. The effective LET at angles other than normal incidence is larger because the particle traverses a larger path length in the semiconductor junction. Thus, if the threshold LET exceeds the effective LET of iron at more extreme angles (≈80 MeV-cm^2/mg), the error rate will be low, Note that unlike total dose effects, shielding is not effective for SEU effects from galactic cosmic rays because of their extremely high energy.

SEU Error Probability. In order to calculate the expected error rate, three different relationships are required:

- The expected distribution of particles vs. LET,
- The cross section for upset or latchup as a function of LET, usually obtained from laboratory measurement, and
- A calculation of the expected error rate that combines the first two relationships with a calculation of the effect of the omnidirectional particle flux on the charge produced in the device by the incident particles. Computer programs are available that perform this calculation. The net result is a fixed number for the upset or latchup probability.

The error rate is often expressed in errors per bit day. The error rate of hardened devices can be on the order of 10^{-8} errors/bit-day or lower. The error rate of unhardened devices is generally several orders of magnitude greater.

Single-Event Phenomena in Devices

Single-Event Upset. As discussed above, a high-energy ion induces a short-duration pulse of current in a p-n junction, such as the drain region. If the charge collected at the drain of a CMOS storage element (e.g., memory or flip-flop) exceeds the critical charge required to switch the circuit, it will change state, and the information that was previously stored will be lost. The circuit still functions normally, and can be reset to its original configuration by reinitializing or rewriting it. In a complex circuit, SEUs will appear at random locations, depending on the particular region that is struck by a high-energy particle. The term SEU describes the situation where the passage of the particle through the device produces only a single upset.

Originally, SEU effects were caused only by heavy ions. However, as individual transistors were scaled to smaller dimensions in order to increase the size and complexity of VLSI circuits, their susceptibility to SEU effects increased. If the sensitivity increases sufficiently, devices can be upset with protons (through nuclear reactions) as well as with heavy particles. [8] This increases the upset rate by many orders of magnitude because of the large number of protons in solar flares and in trapped radiation belts.

Multiple-Bit Upset. For some technologies, such as DRAMs or certain SRAMs, the ionization track from a single particle may cause several storage elements in a circuit to upset .[9] This is called multiple-bit upset. It is more difficult to deal with than SEU because the multiple errors may interfere with system-level approaches such as error-detection-and-correction (EDAC) that are often used to overcome SEU effects.

Single-Event Transients. In addition 'to the effect on storage cells, single-event interactions can produce transient output pulses in combinational logic circuits that do not contain internal storage elements.[10] These transients are usually of short duration (≈ 1 ns), but may indirectly produce changes in the state of other circuits if they occur at critical time periods (such as during clock or data transitions).

1 :rror Detection and Correction. One frequently used approach to harden a system to SEU effects is the application of EDAC, which can be implemented in several ways, and can be a very effective way to accommodate SEU-induced errors in memory, microprocessor, or interface blocks. Some EDAC approaches are limited to detection of single errors in a specific word, while others can detect and correct for multiple word errors. In order for EDAC to be effective, the error rate must be low enough so that the fraction of the time that the EDAC is correcting is within the allowable time window, and the probability of multiple-bit errors must be sufficiently low.

Single-Event Latchup. Bulk CMOS designs contain two parasitic bipolar transistor structures that form a four-layer structure, similar to a silicon-controlled rectifier. These bipolar structures are not involved in normal operation of CMOS devices, but can be inadvertently triggered into an "on" condition by transient signals at the input or output terminals. All CMOS designs use special guardbands and clamp circuits at 1/0 terminals to prevent this from happening in standard circuit applications.

However, in a radiation environment transient signals are no longer confined to 1/0 terminals, and it is possible for the current pulses from heavy ions to trigger latchup in *internal* regions of a CMOS device as well as at 1/0 circuitry. [11] Once latchup occurs, the four-layer structure will be switched into a conducting mode, and will remain in that mode until power is removed. Currents during latchup can be very high. In most circuits currents of several hundred milliamps or more will flow in the localized region where latchup is triggered, rapidly heating that section to extremely high temperatures.

Because of the potential for catastrophic damage, latchup is a very serious problem for space systems. The most conservative approach is to test samples of each device type, anti disallow use of any device that exhibits latchup. A number of methods have also been proposed to overcome latchup at the system or subsystem level by sensing excess current, which is a signature of latchup, and temporarily removing power. However, the power must be removed within a few milliseconds after latchup occurs in order to avoid possible catastrophic damage to the device metallization or bonding leads.

Radiation Testing for Latchup. Latchup is affected by many variables, including the bias conditions that are applied during testing. Latchup tests should be made under conditions of maximum power supply voltage. Another important variable is temperature, At 125 C the threshold LET for latchup decreases by about a factor of three compared to its value at room temperature. [12] Therefore, latchup testing must be done at the highest temperature required in the application. A null latchup result at room temperature cannot provide any direct information about the likelihood of latchup at higher temperatures.

Heavy-ion latchup testing is done using a particle accelerator, placing the device in a vacuum chamber that is connected to the accelerator. Latchup is detected by monitoring both the power supply current and functional operation of the circuit, The range of ions used for latchup testing should be 40 μm or more in silicon.

Analog-to-Digital Converters

Numerous advances have been made in the design of precision analog-to-digital converters which have increased the precision and accuracy of these devices. In order to meet electrical specifications, matching of internal components must be maintained to levels of a few hundred microvolts or less, which makes these devices sensitive to second-order effects that are not important in applications with less stringent specifications. Consequently, testing and qualifying these devices for space is a difficult problem.

Three examples will be discussed, which are all commercial, unhardened designs: (1) a 12-bit BiCMOS design; (2) a 14-bit CMOS design, which uses conventional technology; and (2) a 16-bit CMOS design, which incorporates extensive digital circuitry that provides internal self-calibration, The latter design must be treated as a subsystem because it contains an internal microprocessor, memory, and numerous digital functions which can potentially malfunction in unusual ways when the device is exposed to radiation. In order to use this

device successfully, methods of verifying correct operation and resetting the device must be included in the application architecture.

BiCMOS Converter

The 12-bit BiCMOS device uses bipolar devices for critical analog applications which demand close matching and low input offset voltage (such as the reference amplifier and comparator), but uses CMOS technology in input/output circuitry and in the successive-approximation register. In order to meet the higher voltage requirements of typical A/D applications, the gate oxide is much thicker than the gate oxide used in digital CMOS technologies. The main radiation concerns are total dose damage, which may degrade the accuracy; and ensuring that latchup cannot occur when the device is exposed to heavy ions.

Radiation testing showed that the conversion accuracy remained well within specification until catastrophic failure occurred, but that the tri-state output leakage current increased substantially at low levels. The failure mode is caused by threshold shift in the digital CMOS output circuitry; [13] the failure level is consistent with the gate oxide thickness of the technology.

As shown in Figure 3, the results depended strongly on the dose rate used for testing, and the device could be used at levels above 15 krad(Si) at low dose rates. High-temperature biased annealing tests were done on irradiated devices to ensure that partial compensation by interface states was not a factor. The part was approved for use in the system, requiring lot-sample tests of the radiation response at low dose rates to assure that production devices remained within the limits.

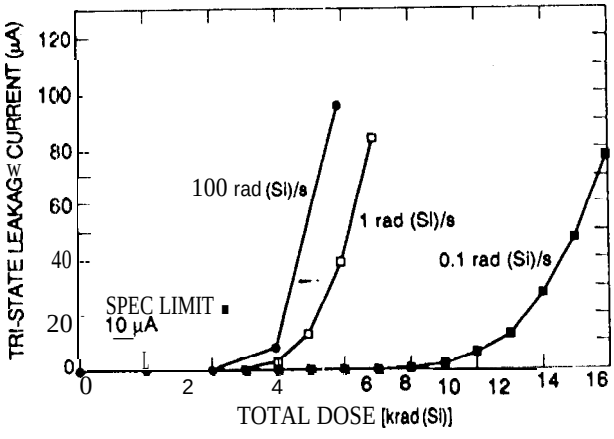

Figure 3. Tri-state leakage current vs. total dose for 12-hit BiCMOS A/D converter

Latchup testing was done at high temperature, using heavy ions from a high-energy accelerator. The device did not latch in any tests, and used an n-substrate which generally reduces latchup susceptibility. The maximum effective LET ion used in the test was 110 MeV-cm^2/mg, which is sufficiently high so that the probability of' latchup is negligible for most space applications,

14-Bit CMOS Converter

Total dose degradation of this device was also strongly dependent on dose rate. At 65 rad(Si)/s, the device would no longer execute conversions after exposure to ~1 krad(Si), a very low level. No significant changes in converter accuracy occurred prior to catastrophic failure.

When tests were done at lower dose rates (≈1 rad(Si)/s), the device did not fail until approximately 20 krad(Si), a substantial improvement that is probably due to annealing of hole traps in the CMOS section. At low dose rates, the dc parameters associated with converter accuracy (i.e., incremental and differential nonlinearity) still remained within specification after total dose irradiation until the device failed catastrophically. However, the signal-to-noise ratio degraded significantly, as shown in Figure 4. The increase in noise degrades performance when the device is used dynamically, ant! decreases the effective conversion accuracy to approximately 11 bits at full frequency after the device is exposed to 40 krad(Si).

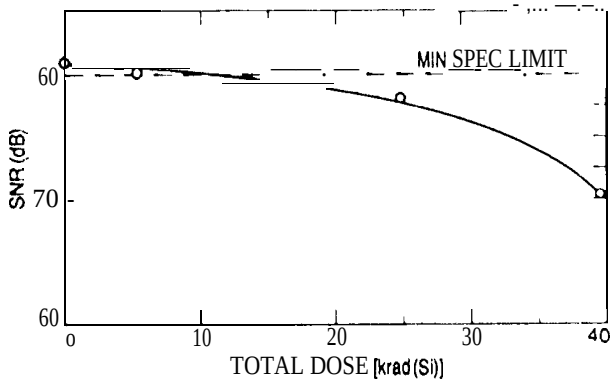

Figure 4. Increase in current noise with total dose for a 14-bit CMOS A/D converter.

Because this device failed catastrophically at such low levels, there was too much risk in assuming that annealing could allow its use in space at levels above 20 krad(Si), even though laboratory tests indicated that the part might be acceptable. Instead, the part was procured in a special package that incorporated spot shielding, reducing the total dose level to acceptable levels for this part. lot-acceptance testing was also required.

High-Accuracy CMOS Converter

The 16-bit CMOS A/D converter uses CMOS circuitry, and is extremely complex. The accuracy is achieved by providing complex internal digital functions that correct for small deviations in internal component matching, as well as temperature, and provide internal

self calibration, This feature introduces many possible failure modes that are not present in more conventional designs. Consequently. single-event upset is a major concern for this technology.

SEU testing was done at a high-energy accelerator. Latchup was not observed, even at elevated temperature, However, the device upset during SEU tests with two separate failure modes. The threshold LET for the digital section of the device was 8.4 MeV-cm^2/mg. Although some single errors were detected, in many cases bursts of more t hart 4000 errors were pi educed by the interaction of a single ion with the device. This is particularly significant because if the errors extend beyond the time required to implement internal calibration, the device can only be restored to normal operation by temporarily interrupting power. Thus, even though latchup did not occur in this device, the presence of the complex digital circuitry could cause the device to switch into failure modes that require power sequencing in order to allow recovery. Upsets were also detected in the analog section, The threshold LET for analog upsets was approximately 38 MeV-cm^2/mg.

Even though this device was extremely attractive to designers because of its accuracy and internal features, it was rejected for space use because of the difficulty of coping with the complex SEU response,

Memories

The density of storage elements in semiconductor memories has increased dramatically in recent years, and this has affected both ionization damage and single-particle effects.

For devices with feature sizes above 1 µm, the total dose hardness has actually increased somewhat because of reduction in gate oxide thickness imposed by scaling. Current devices with feature sizes of 1.2 µm have oxide thicknesses of about 220 A. Figure 5 shows a calculation of the expected failure level as oxide thickness decreases. However, corresponding reductions have not been made in the thickness of field oxides, and for this reason the total dose hardness of present semiconductor memories is generally limited by field-oxide inversion, which causes large increases in power supply current. Figure 5 also shows the approximate transition region between gate oxide and field oxide failure, Semiconductor memories have generally followed this trend.[14] However, as discussed later in the section on future trends, there are additional factors in submicron memories which may cause them to deviate fron i these trends.

Scaling effects have generally increased the sensitivity of semiconductor memories to SEU because the critical charge required to change the state of memory cells has decreased. The threshold LET of typical 1 Mbit SRAMS is in the range of 5-9 MeV-cm^2/mg.[15] DRAMs have even lower threshold levels.

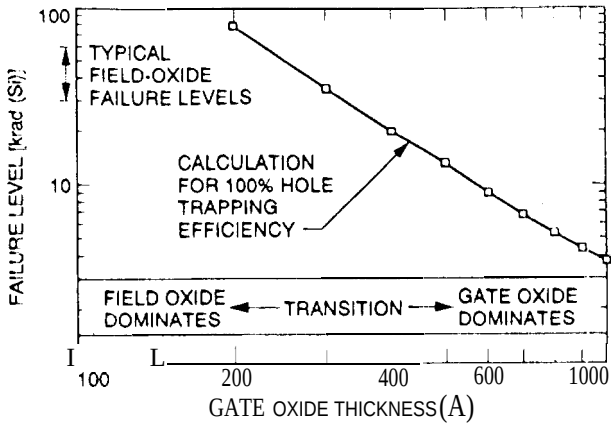

Figure 5. Failure levels of CMOS devices as a function of gate oxide thickness. Note that field oxide failure dominates for devices with thin gate oxides.

Latchup sensitivity has also increased as devices are scaled to smaller dimensions. However, some commercial devices are made on low-resistivity substrates, which increase the threshold LET for latchup to much higher values. [16] Some devices fabricated this way are actually immune to single-particle latchup. This provides an effective way to select devices that are relatively immune to latchup, overcoming one of the major barriers for commercial memories in space applications.

Even though dynamic memories are extremely sensitive to SEU, it is still possible to use them in space systems. One recent application at JPL required very large memory on a spacecraft, precluding the usc of more SEU-resistant devices because of their smaller size. The total system required 2.5 Gbits of memory, and 640 4-Mbit commercial DRAMs were used in the design.

Figure 6 shows the SEU cross section for these devices, Note that the threshold LET is extremely low, which makes this device susceptible to upset from protons as well as heavier particles, and results in a high rate of SEU errors for the total system.

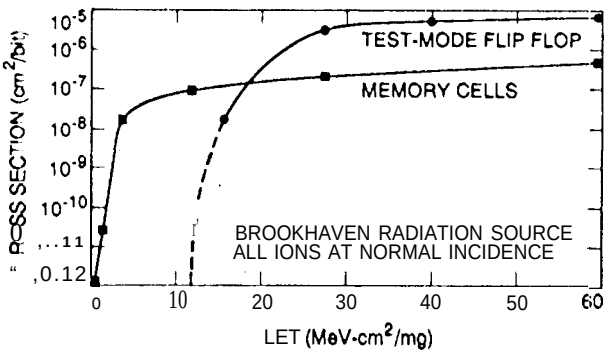

Figure 6 Single-event upset cross section of a 4-Mbit DRAM

To overcome the high SEU rate, error detection and correction were used, along with aluminum shielding, that reduced the number of errors from protons. The error correction scheme reduced the number or errors within the memory system by about four orders of magnitude, which was an acceptable level.

Microprocessors

Microprocessors are difficult to evaluate for space applications because of their complexity, which makes testing costly and involved; and because the results of radiation testing may depend on the particular application. In general, total dose testing is more straightforward, and will not be discussed here, even though there are unique difficulties associated with total dose effects in these devices. [17] The following discussion will address single-event phenomena in these devices

Single-event effects in microprocessors are particularly difficult to deal with because the device can only be tested in a very limited number of conditions, with the distinct possibility that some critical failure modes may be missed. From an application standpoint, users are concerned with two distinct problems: first, determining the expected error rate in the application, and second, establishing the likelihood of errors that cannot be reset through normal electrical procedures, but require a "cold boot" after temporarily removing power from the device, The latter en or condition could prevent normal recovery from single-event upset, and could occur if a single-particle transient places the microprocessor in a memory or address location that is outside the range expected by software. Thus, cold-boot problems are strongly dependent on application software.

The single-event error rate also depends on the particular software that is running during the time that the part is tested. For example, Figure 7 shows the dependence of the single-event cross section on operating conclitions.[18] Note the large difference in cross section that occurs when the device is operated in different modes. Although the threshold LET for upset is not affected, the saturation cross section can vary by more than a factor of 30 in different applications. This not only introduces ambiguity in test results, but can have a major impact on the importance of upset in applications because of the difference in the saturation cross section between different operating conditions.

One approach that has been used to standardize test results is register testing, which uses a register-intensive instruction set. [19] A block diagram of a register test approach is shown in Figure 8. This approach assumes that register errors are the dominant source of single-event upsets, and uses a machine language program that continuously checks and corrects for register errors. This method provides more standard test results, but does not address the issue of recovery from SEU effects in complex applications. Nevertheless, the cross section

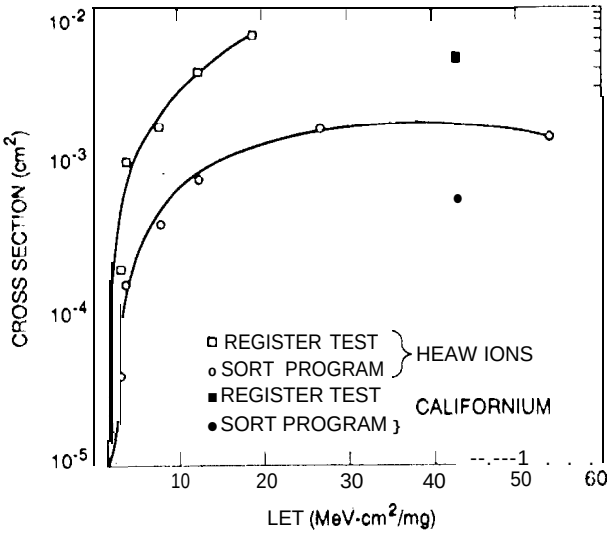

Figure 7. Dependence of microprocessor SEU cross section on operating conditions,

that results from register testing is generally higher, so that it can be used to provide an upper bound estimate of the error rate in more general applications,

The 80C186 microprocessor is a good example of application of commercial technologies in space. Even though this device has a large chip area (≈ I cm²), the area of the chip that is devoted to internal registers is very small. There are 70 registers, with a total of 713 bits. Thus, the net SEU cross section is small compared to that of a memory with the same chip area,

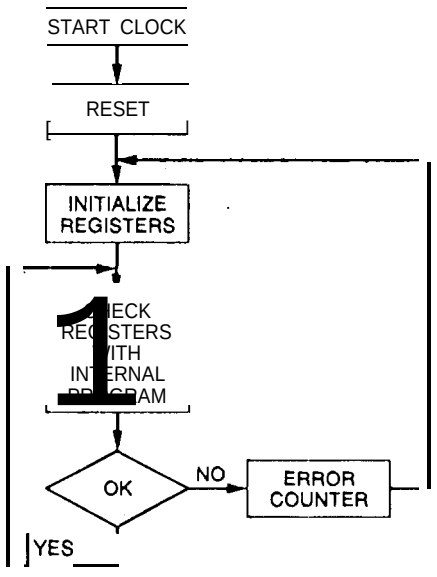

Figure 8. Block diagram of register test approach for microprocessor SEU testing.

SEU test results using a register test approach are shown in Figure 9.[20] The cross section results are presented in cm^2/bit, and the effective cross section in an application would depend on the particular way (hat the device was used. The limiting value of the saturation cross section can be calculated by simply multiplying the results in Figure 9 by 713, the total number of internal register bits.

As shown in Figure 9, this device contained two different types of registers with different geometries, and hence different SEU responses. The data control registers had a lower threshold I. ET, with a saturation cross section that was approximately twice the saturation cross section of the registers that were directly involved with internal microprocessor operations. The threshold LET is sufficiently high that no upset is expected from protons.

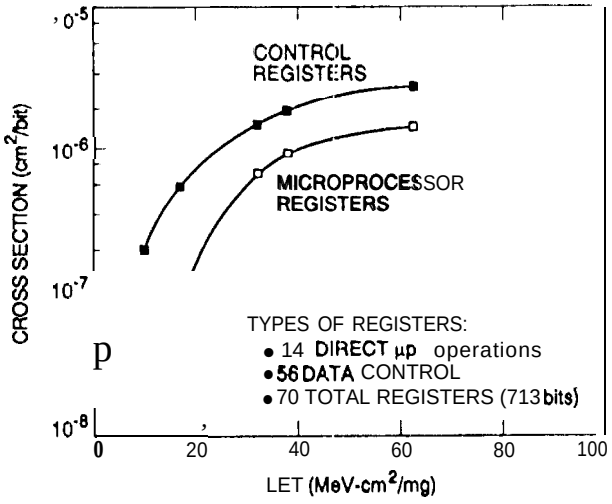

Figure 9. SEU test results for the 80C186 microprocessor.

Not all registers were used in the application, a space probe, and this information was used to calculate the effective saturation cross section. GCRand solar flare heavy particle spectra were used to calculate a range of error rates, depending on solar flare activity. The most likely error rate was estimated as 2.4×10^{-3} errors per bit day, which is approximately one error per year. Solar flare activity could increase the error rate by approximately a factor of 20, but this rate was still acceptable in the system. Note however that even though the SEU rate was low for the microprocessor, much larger SEU rates occurred for memories. This required periodic scrubbing of the memory system to correct for soft errors.

Future Trends: Effect of Scaling and Technology Changes

Scaling and technology evolution have had major impacts in radiation hardness in the past, and will continue to be important in the future. However, it is difficult to accurately predict future technology directions, so there is some uncertainty in any prediction of technology evolution, Recent trends provide some insight into likely changes in the near term.[21,22]

Total Dose Damage in Scaled Devices

Previous work on MOS devices has shown that gate oxide threshold shifts are expected to scale as the square of the gate oxide thickness, with the result that one expects scaled devices to be less affected by total dose damage because of the reduced dimensions.

However, recent work on scaled devices has shown that they are actually more sensitive to total dose than older devices. For example, Figure 10 compares the failure level of three different DRAMs.[23] Two of the devices are from the same manufacturer, and show increased sensitivity with reduced feature size. The third device is from a different manufacturer, and uses a lower internal supply voltage (3.6 V) for the memory cells. The important point is that other factors are important in device scaling, including internal circuit margins, which may cause real devices to behave differently than elementary scaling theory based on test structures.

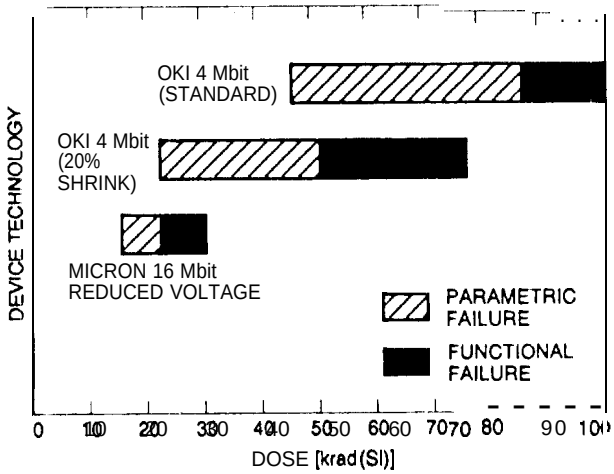

Figure 10. Total dose failure levels of advanced memories with submicron feature sizes.

Single-Event Herd Errors

An important new effect was reported in 1992, when permanent errors were found in semiconductor memories after they were subjected to single-event testing. [24,25] The number of hard errors was very small, ranging from about 4 to 50 cells in a 1 Mbit static memory. The number of observed errors was nonlinear with fluence, and the errors could be annealed by either high temperature or exposure to ultraviolet light. The results were consistent with a mechanism corresponding to statistical distributions of localized total dose within the sensitive gate regions of selected devices within the memory array. Thus, these errors appear to be caused by the highly localized deposition of charge from a small number of ions. These effects became significant because the dimensions of the gate of tbe memory cells was sufficiently small that individual devices could be

affected by trapped charge from a single interaction of heavy ions instead of the aggregate charge from very large numbers of ions. Additional experimental results have been obtained with DRAMs which are similar to the SRAM results.

This is an excellent example of the types of new phenomena that can result from device scaling. It affects designs that depend on large internal impedances such as SRAMs with four-transistor memory cells, and DRAMs, but not devices with active loads (such as 6-T SRAMs). It is an important effect, but there are system solutions such as error checking and correction that can be used to deal with hard errors in applications.

Single-Event Upset Sensitivity

Finally, as device geometry is reduced, less charge is required to upset devices. In general, this causes the threshold LET of unhardened devices to decrease, which increases the SEU error rate because the number of heavy particles increases for low LET. SEU data over the last five years has generally reflected this trend,[15,26,27] although there are large variations between devices because of differences in internal design.

Once. the threshold LET drops to the point that protons can cause upset, the SEU rate increases dramatically because the number of protons in a typical space mission is much larger than the number of heavy particles. In addition to SEU, proton-induced latchup has been observed for some devices with small feature size.

Thus, the general trend is for increased sensitivity to radiation effects as devices are scaled to smaller feature sizes. However, it is still possible to apply these devices in space by using combinations of shielding for total dose effects, and error correction for single-event upset effects, Latchup is the most difficult problem to deal with, but many modern devices are fabricated on low-resistivity substrates with epitaxial layers that make devices more resistant to latchup. It is often possible to select devices which are immune to single-event latchup by a combination of electrical evaluation and radiation testing.

Conclusions

This paper has discussed basic radiation phenomena in integrated circuits, along with examples of their effects in three basic types of devices.

At the present time, commercial devices can be applied successfully in many space applications even though they are susceptible to upset and permanent damage. The key to success is thorough testing and characterization of devices, as well as an understanding of the various effects, particularly phenomena that are more important for newer technologies, such as latchup, SEU, and single-event hard errors. It is often possible to implement system architectures that can correct for transient effects, with selective shielding for devices that are sensitive to total dose degradation, This approach provides a practical, lower cost alternative 10 designs that arc restricted m specialized, hardened parts, and is being implemented in a number of current space systems.

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